

Fig. 1

Ain	Bin	XORout
0	0	0
0	1	1
1	0	1
1	1	0

Fig. 2

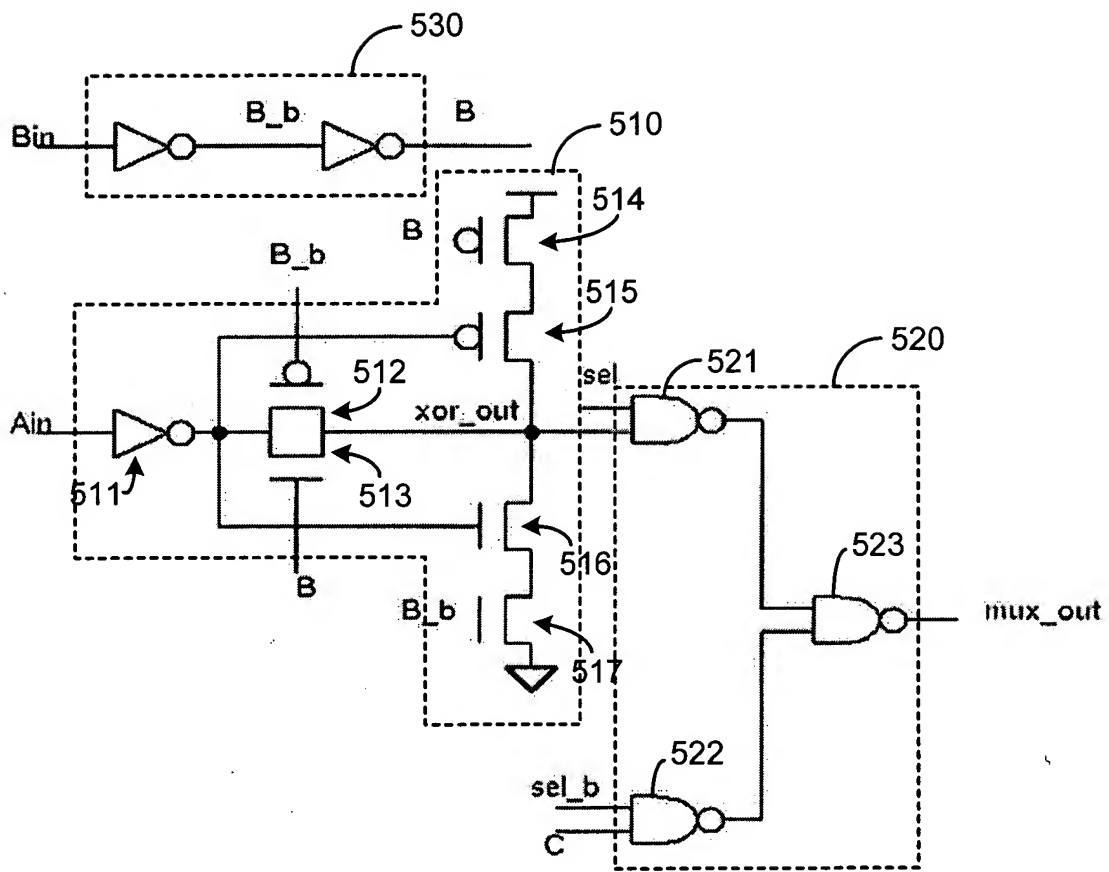
XORout	Cin	Sel	MUXout
*1	*2	0	*2
*1	*2	1	*1

*1 and *2 can be either 0 or 1.

Fig. 3

Ain	Bin	XORout	Cin	Sel	MUXout
0	0	0	*	1	0
0	1	1	*	1	1
1	0	1	*	1	1
1	1	0	*	1	0
*	*	*	0	0	0
*	*	*	1	0	1

Fig. 4



(Prior Art)
Fig. 5

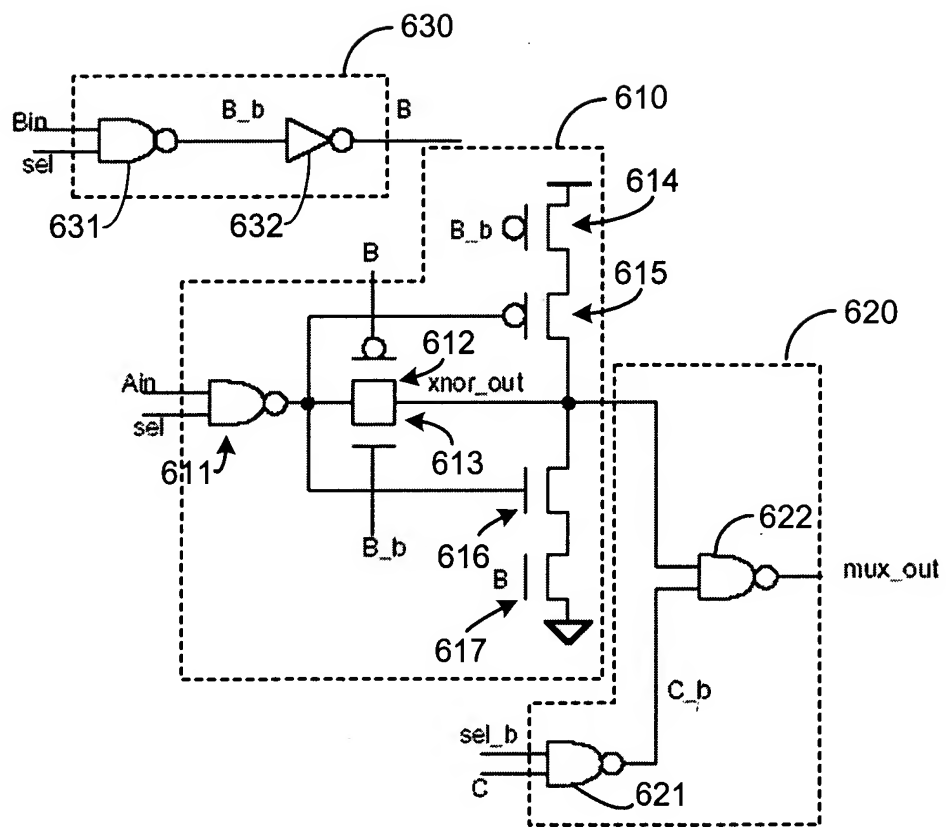
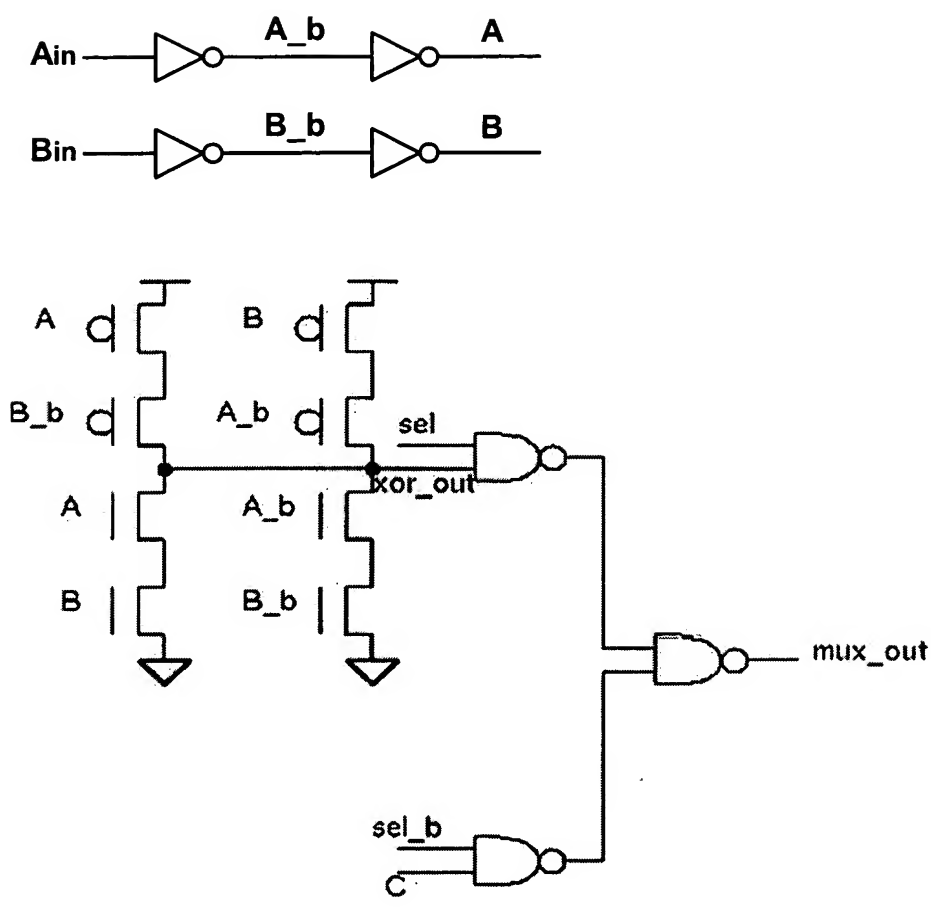


Fig. 6

Ain	Bin	C	sel	A_b	B_b	B	xnor_out	sel_b	C_b	mux_out
0	0	*	1	1	1	0	1	0	1	0
0	1	*	1	1	0	1	0	0	1	1
1	0	*	1	0	1	0	0	0	1	1
1	1	*	1	0	0	1	1	0	1	0
0	0	1	0	1	1	0	1	1	0	1
0	1	1	0	1	1	0	1	1	0	1
1	0	0	0	1	1	0	1	1	1	0
1	1	0	0	1	1	0	1	1	1	0

Fig. 7



(Prior Art)
Fig. 8

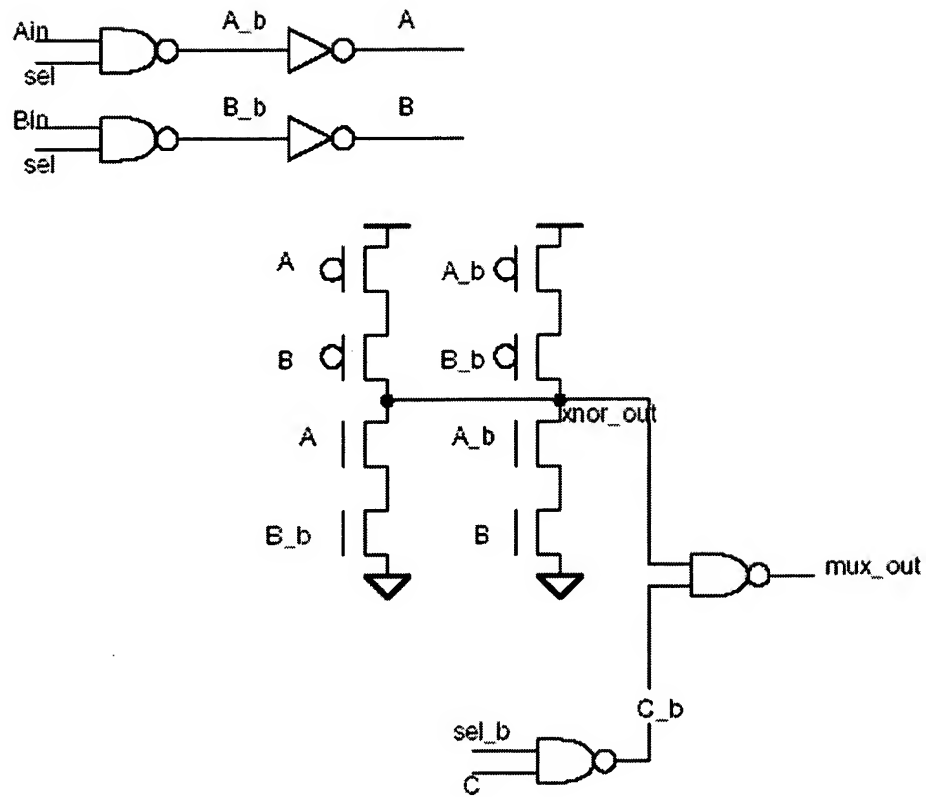


Fig. 9

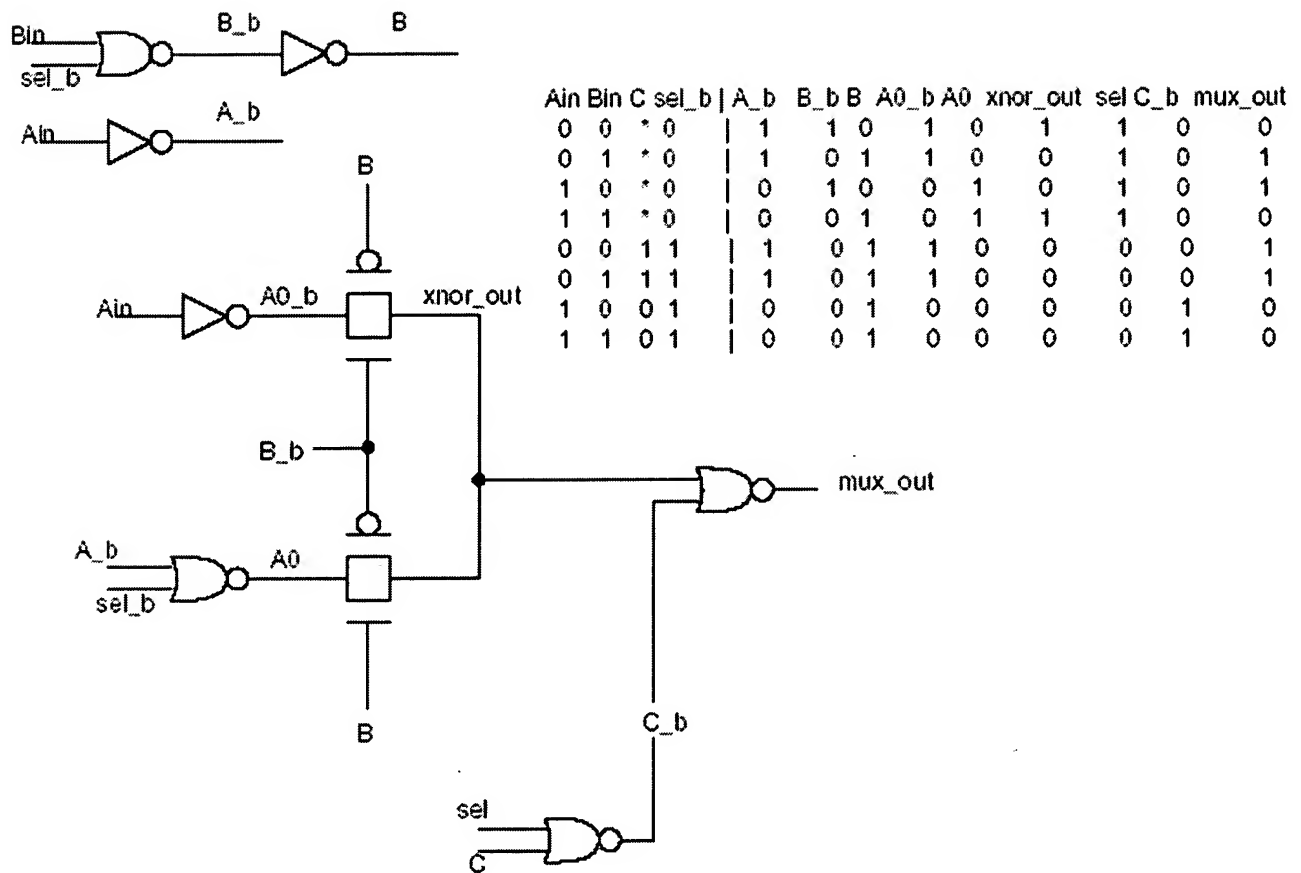


Fig. 10

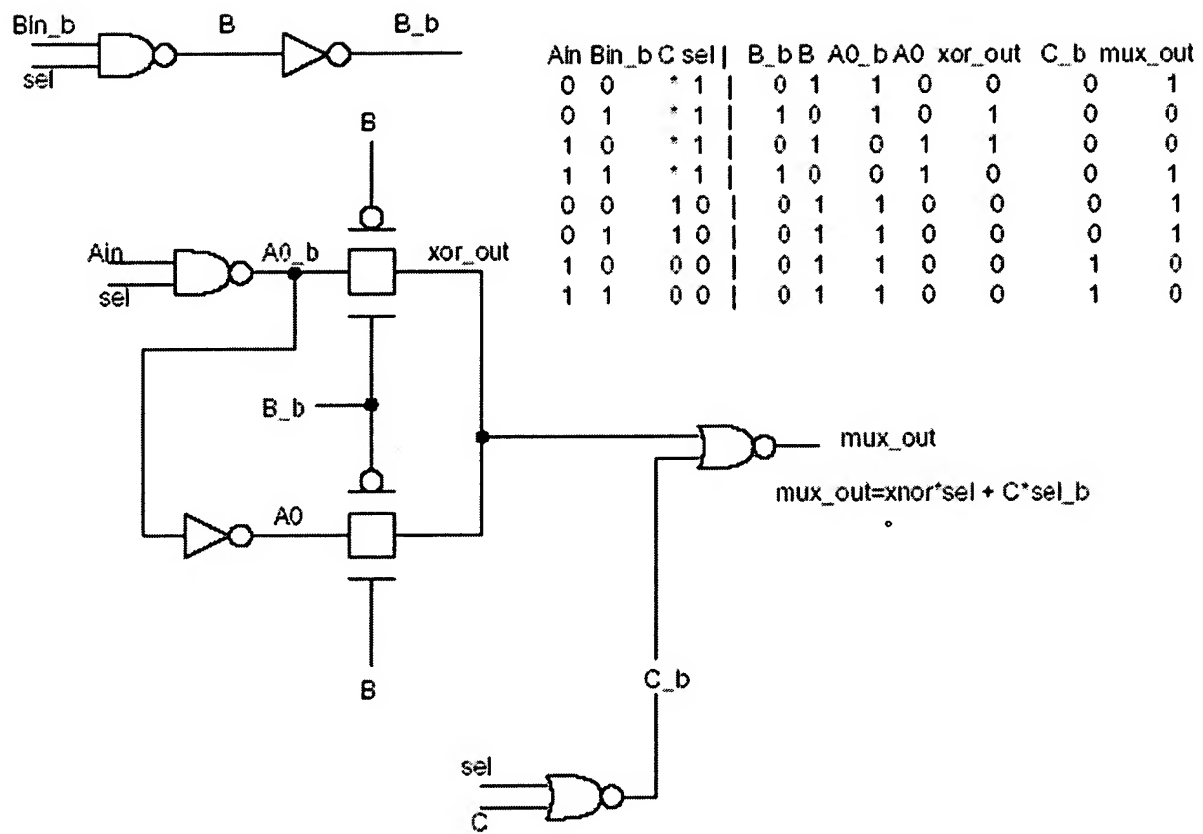


Fig. 11

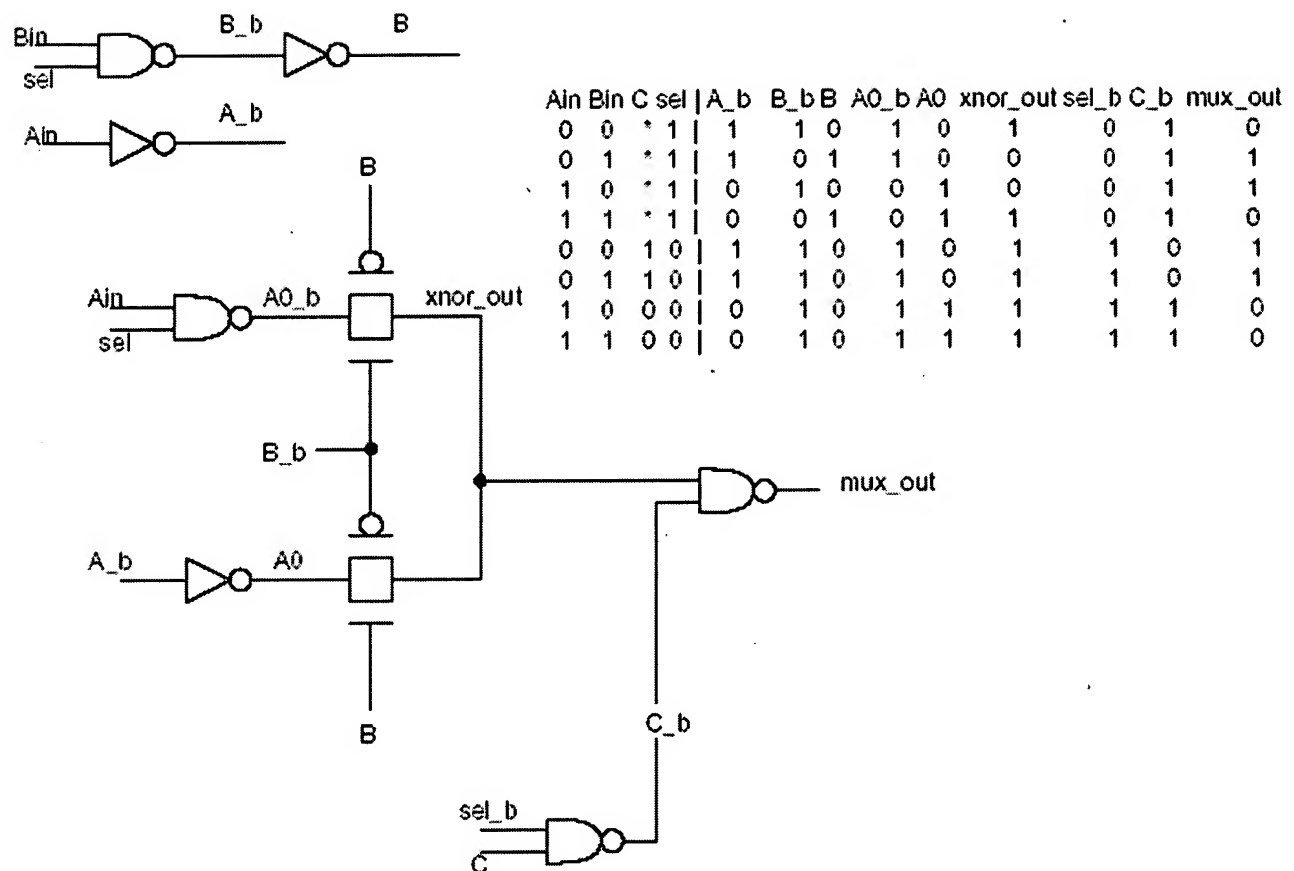


Fig. 12

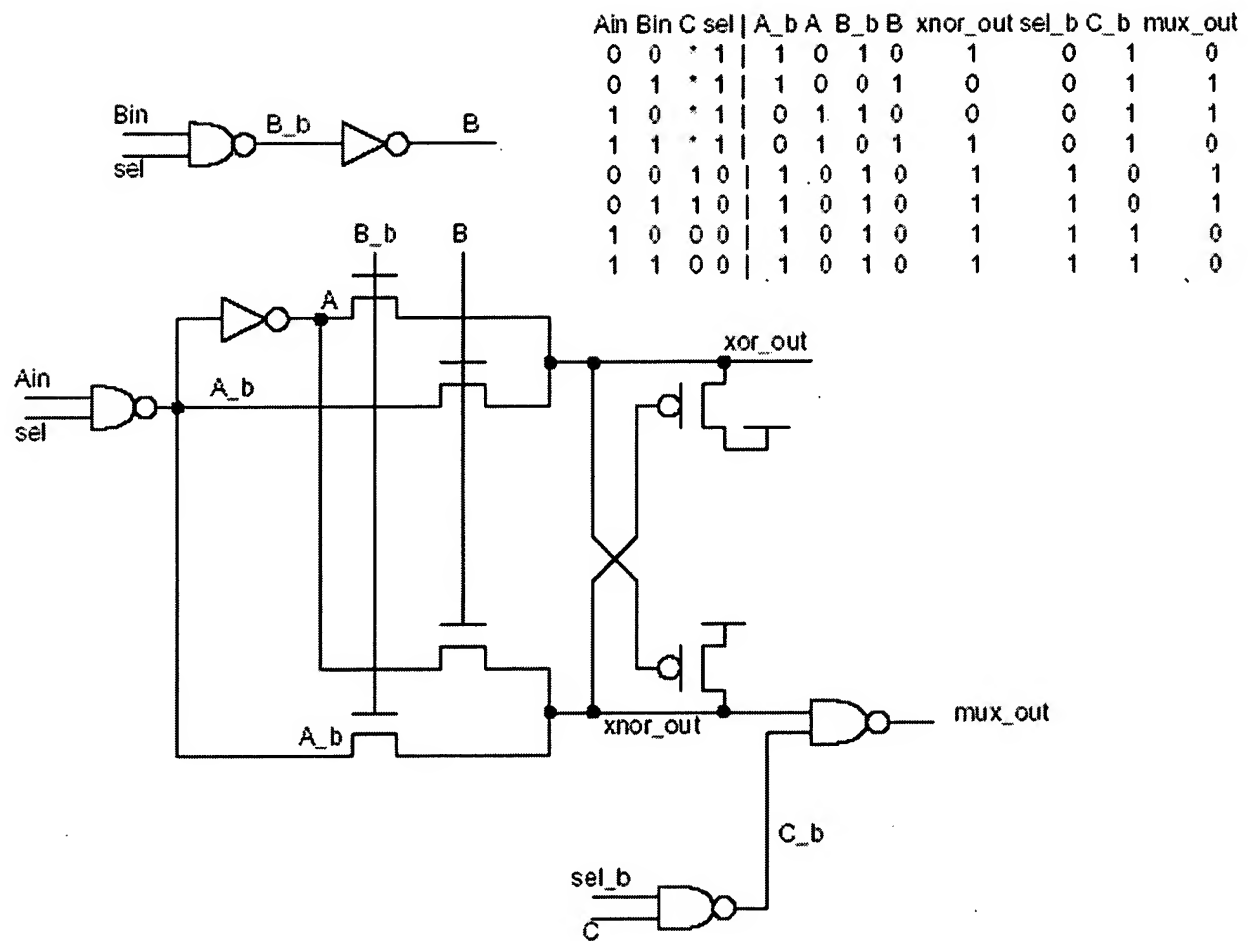


Fig. 13

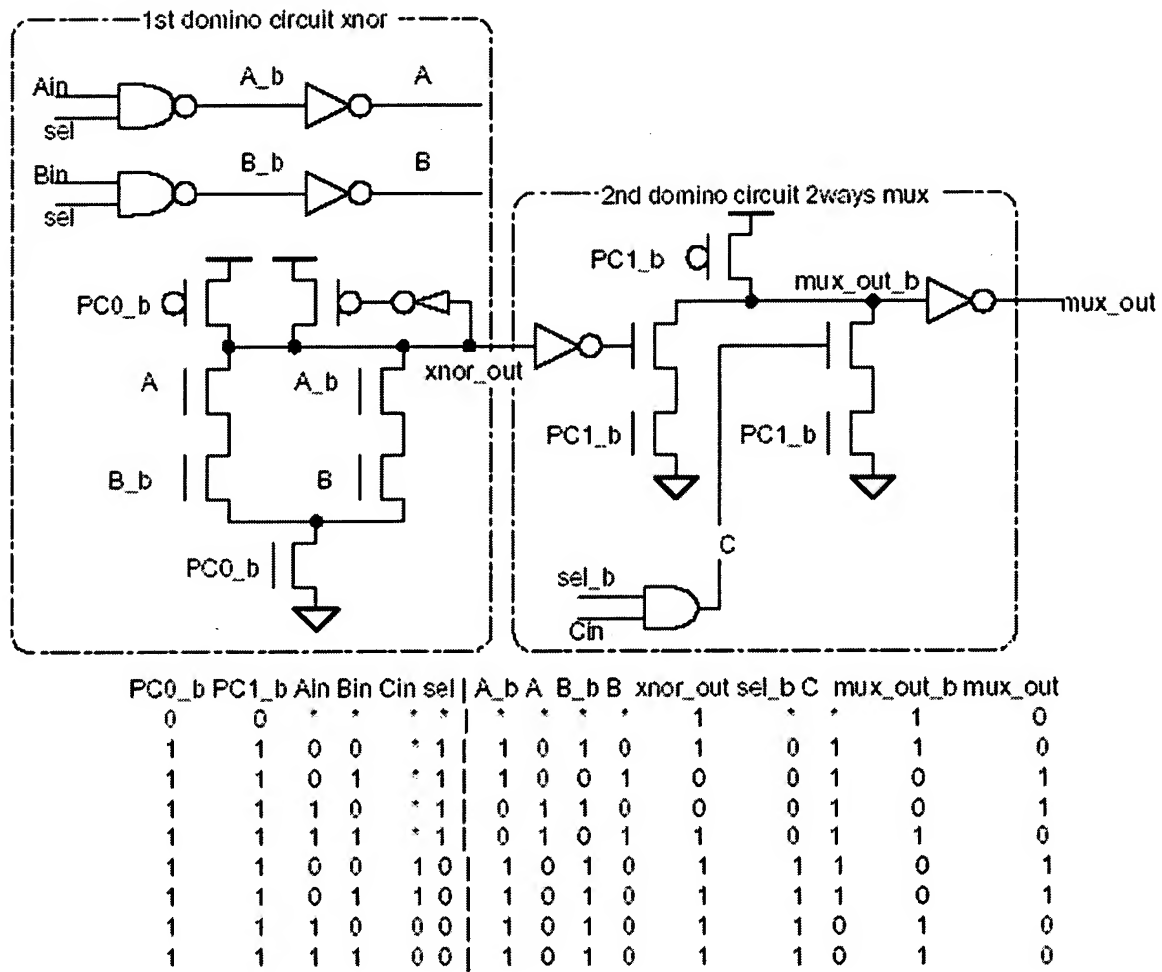


Fig. 14

Ain	Bin	sel0	sel1	sel2	sel3	xnor_out	4ways-mux_out
0	0	1	0	0	0	1	0
0	1	1	0	0	0	0	1
1	0	1	0	0	0	0	1
1	1	1	0	0	0	1	0
*	*	0	1	0	0	1	d1
*	*	0	0	1	0	1	d2
*	*	0	0	0	1	1	d3

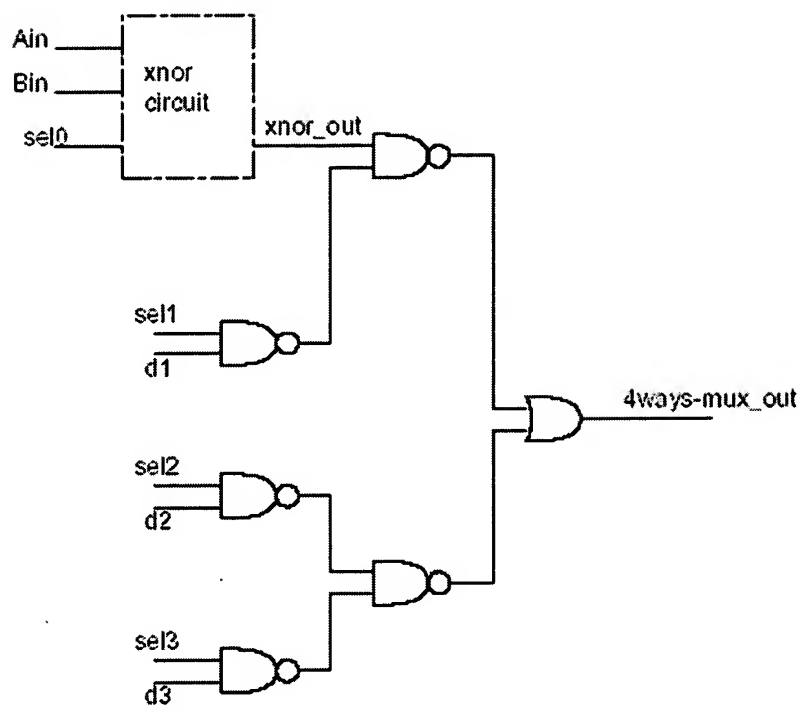


Fig. 15